WN-2343

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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E. Willis
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In re patent application of

Tomohiko Kudo and Naohiko Kimizuka

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

2800

Filing Date: Concurrently Herewith

Examiner: Unknown

For: FABRICATION OF LOW POWER CMOS DEVICE WITH HIGH RELIABILITY



Assistant Commissioner of Patents
Washington, D.C. 20231

## INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following documents listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner. In compliance with the concise explanation requirement under 37 CFR §1.98(a)(3), the relevance of these documents are discussed on page 2 of the subject application. Further, English-language Abstracts are attached to the references.

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481.



Respectfully submitted,

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JP-A No. 11-162973

Abstract:

A pattern is formed on a silicon substrate 10 with photoresist 12. Thereafter, ions to promote the speed in thermal oxidization are selectively implanted thereover. The photoresist 12 is removed and thermal oxidization is then carried out. Thereafter poly-silicon film 18 is grown on an $SiO_2$ film 16 and another pattern is formed. Thus the gate oxide films of MOSFETs with the different thicknesses of $SiO_2$ films are simultaneously formed.

JP-A No. 10-335656

Abstract:

At a time when ions are implanted into the channel region of the MIS-FET, ions for varying the silicon oxide film in formation rate are selectively introduced into an element region where thickness of a gate insulator of silicon dioxide 14 is desired to be relatively thicker or relatively thinner and where a MIS-FET is formed with the desired thickness of the gate insulator. Thereafter, by using a thermal oxidation method or an anodizing method, the gate insulators of silicon dioxide 12 and 14 are formed on the silicon semiconductor substrate 2 so as to have different thicknesses.